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Lin et al.

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(54) **FABRICATION METHODS OF CHIP DEVICE PACKAGES**

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H01L 21/768 (2006.01)
H01L 21/48 (2006.01)
(Continued)

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CPC ***H01L 21/76898*** (2013.01); ***H01L 21/481*** (2013.01); ***H01L 21/76897*** (2013.01); ***H01L 23/3178*** (2013.01); ***H01L 23/5389*** (2013.01); ***H01L 24/19*** (2013.01); ***H01L 24/94*** (2013.01); ***H01L 27/14618*** (2013.01); ***H01L 27/14636*** (2013.01); *H01L 23/3192* (2013.01); *H01L 24/03* (2013.01); *H01L 24/05* (2013.01); *H01L 24/11* (2013.01); *H01L 24/13* (2013.01); *H01L 2224/02372* (2013.01); *H01L 2224/0345* (2013.01); *H01L 2224/0401* (2013.01); *H01L 2224/04026* (2013.01); *H01L 2224/04105* (2013.01); *H01L 2224/05548* (2013.01); *H01L 2224/05567* (2013.01); *H01L 2224/05624* (2013.01); *H01L 2224/05639* (2013.01); *H01L 2224/05647* (2013.01); *H01L 2224/05655* (2013.01); *H01L 2224/06181* (2013.01); *H01L 2224/1132* (2013.01); *H01L 2224/11462* (2013.01); *H01L 2224/11849* (2013.01); *H01L 2224/131* (2013.01); *H01L 2224/13022* (2013.01); *H01L 2224/20* (2013.01); *H01L 2224/94* (2013.01); *H01L 2224/97* (2013.01); *H01L 2924/014* (2013.01); *H01L 2924/01006* (2013.01); *H01L 2924/01013* (2013.01); *H01L 2924/01029* (2013.01); *H01L 2924/01047* (2013.01); *H01L 2924/01075* (2013.01);
(Continued)

(58) **Field of Classification Search**
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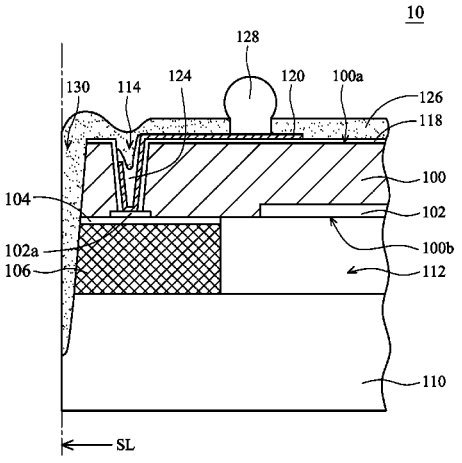
See application file for complete search history.

Primary Examiner — David Vu
(74) *Attorney, Agent, or Firm* — Liu & Liu

(57) **ABSTRACT**

A chip package and a fabrication method thereof are provided. The chip package includes a semiconductor substrate, having a first surface and an opposing second surface. A spacer is disposed under the second surface of the semiconductor substrate and a cover plate is disposed under the spacer. A recessed portion is formed adjacent to a sidewall of the semiconductor substrate, extending from the first surface of the semiconductor substrate to at least the spacer. Then, a protection layer is disposed over the first surface of the semiconductor substrate and in the recessed portion.

19 Claims, 11 Drawing Sheets



(51) **Int. Cl.**

H01L 23/538	(2006.01)
H01L 23/00	(2006.01)
H01L 23/31	(2006.01)
H01L 27/146	(2006.01)

(52) **U.S. Cl.**
CPC *H01L2924/01079* (2013.01); *H01L 2924/12041* (2013.01); *H01L 2924/1461* (2013.01); *H01L 2924/1579* (2013.01); *H01L 2924/15787* (2013.01); *H01L 2924/15788* (2013.01)

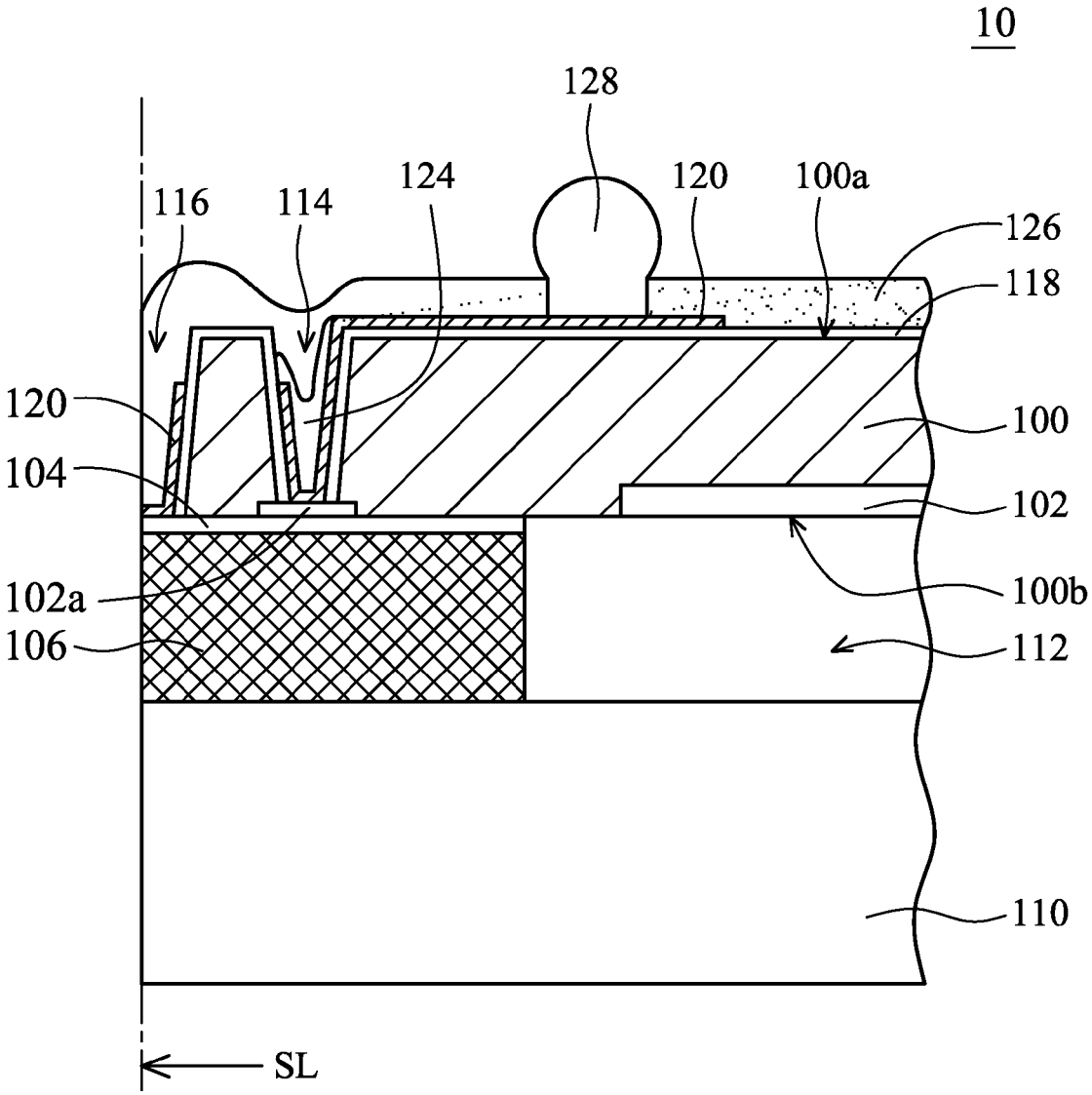

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FIG. 1

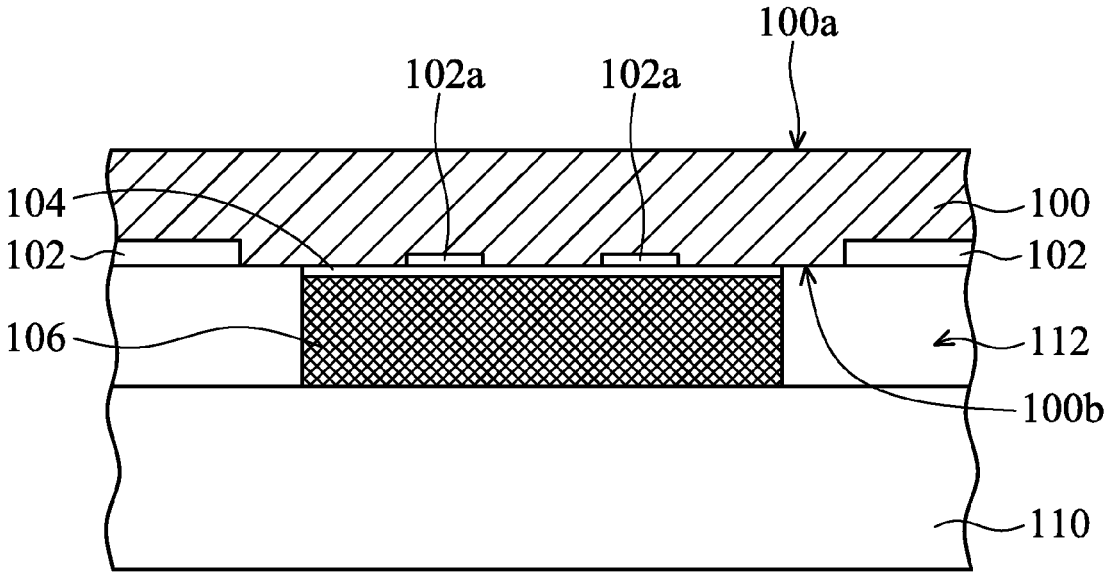
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FIG. 2A

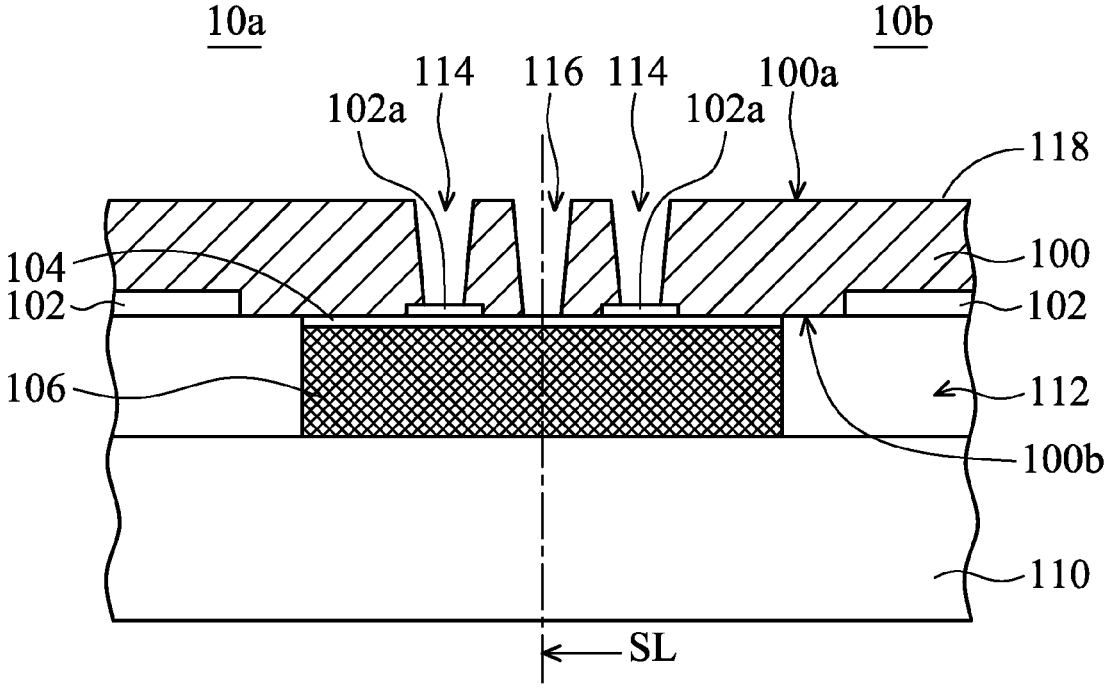
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FIG. 2B

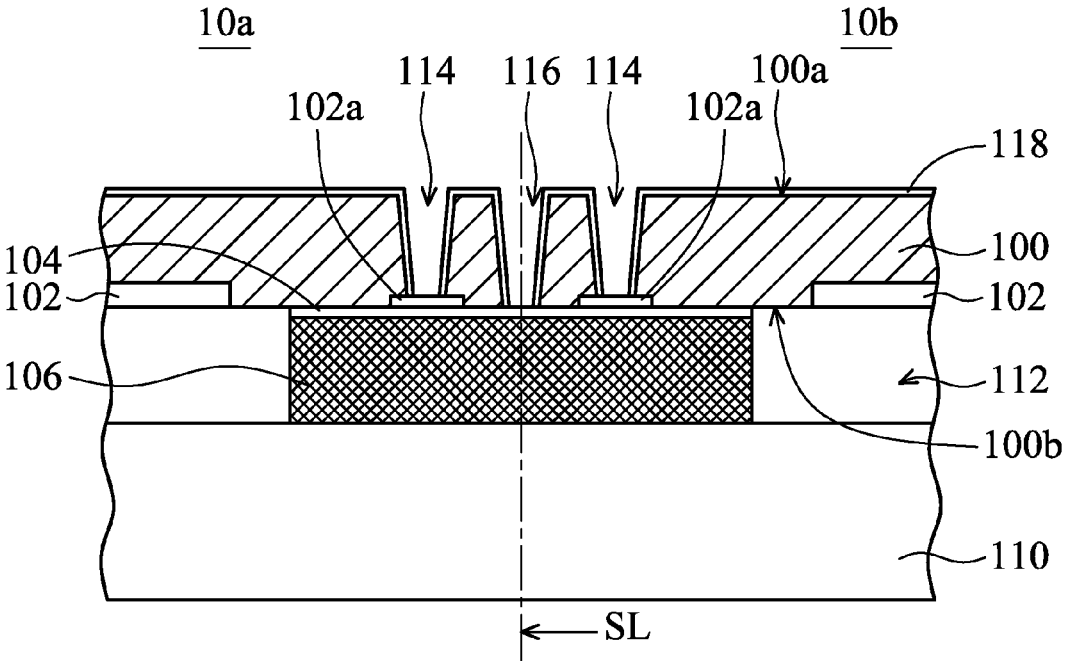
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FIG. 2C

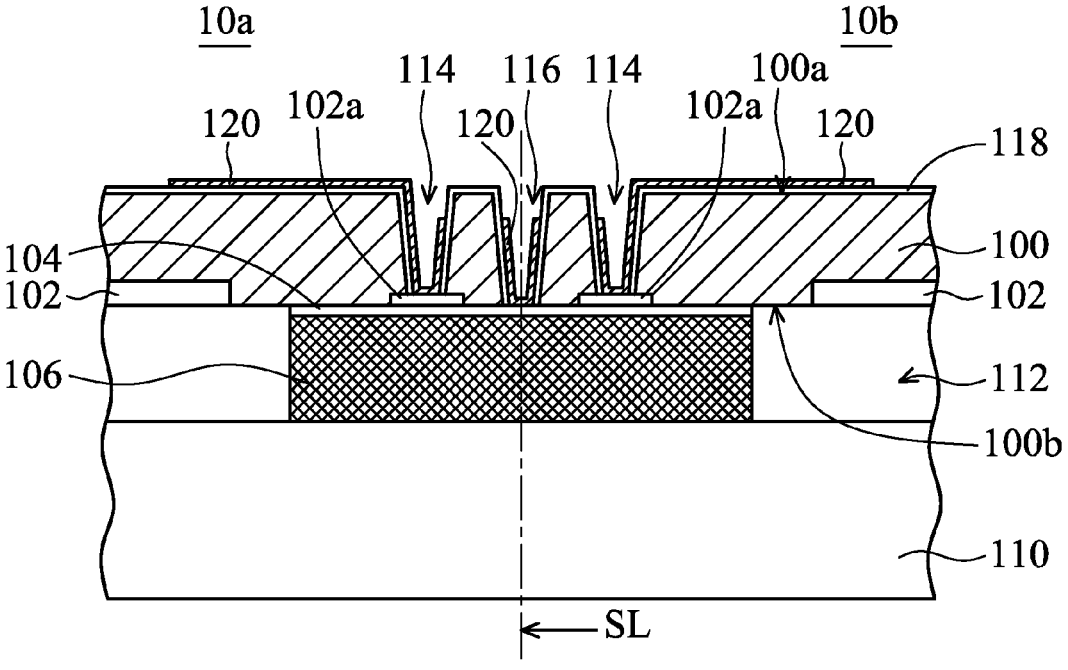
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FIG. 2D

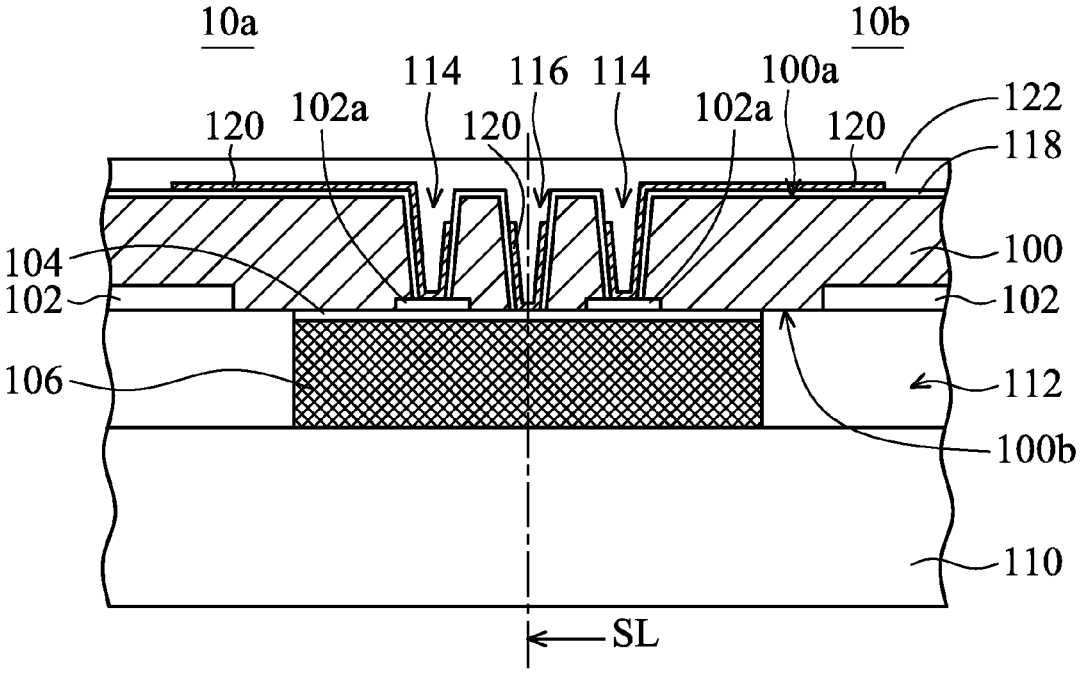
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FIG. 2E

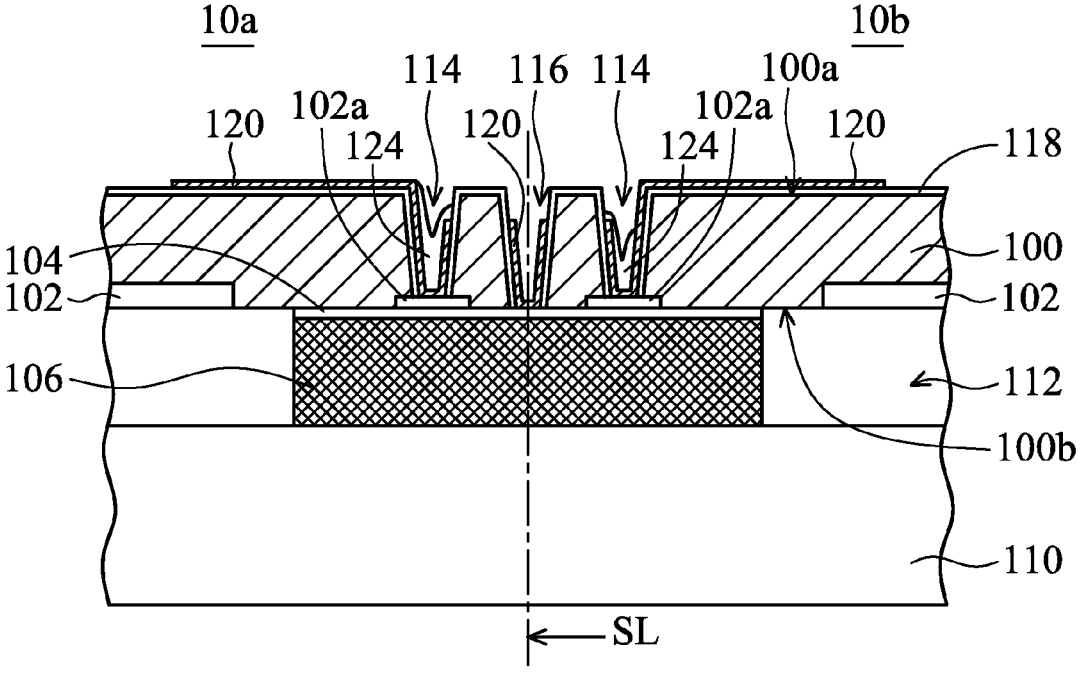
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FIG. 2F

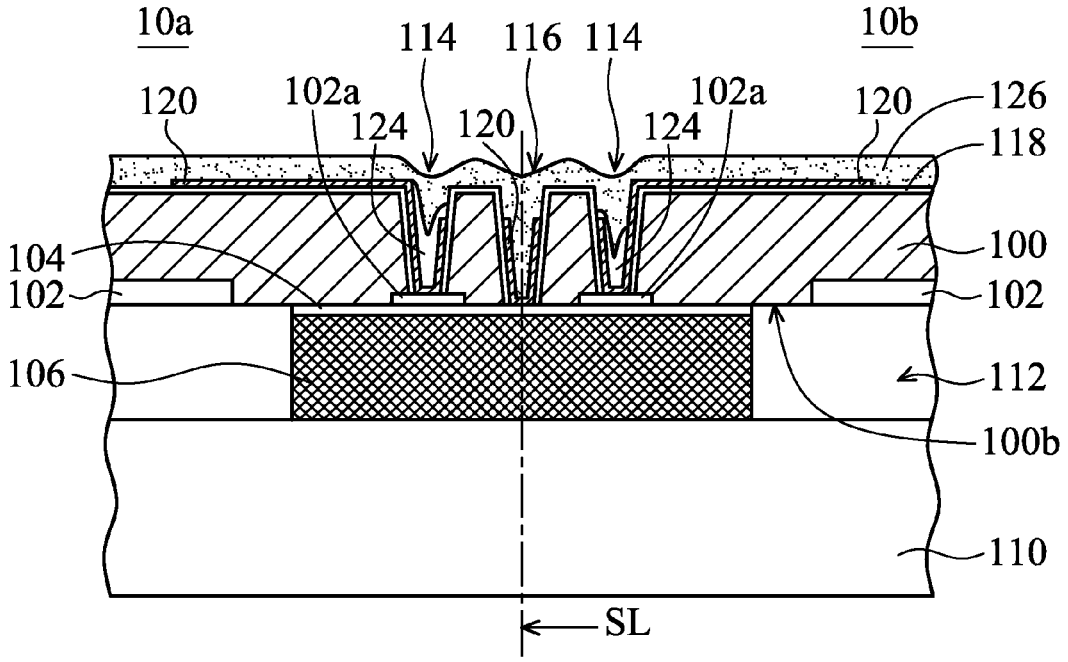
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FIG. 2G

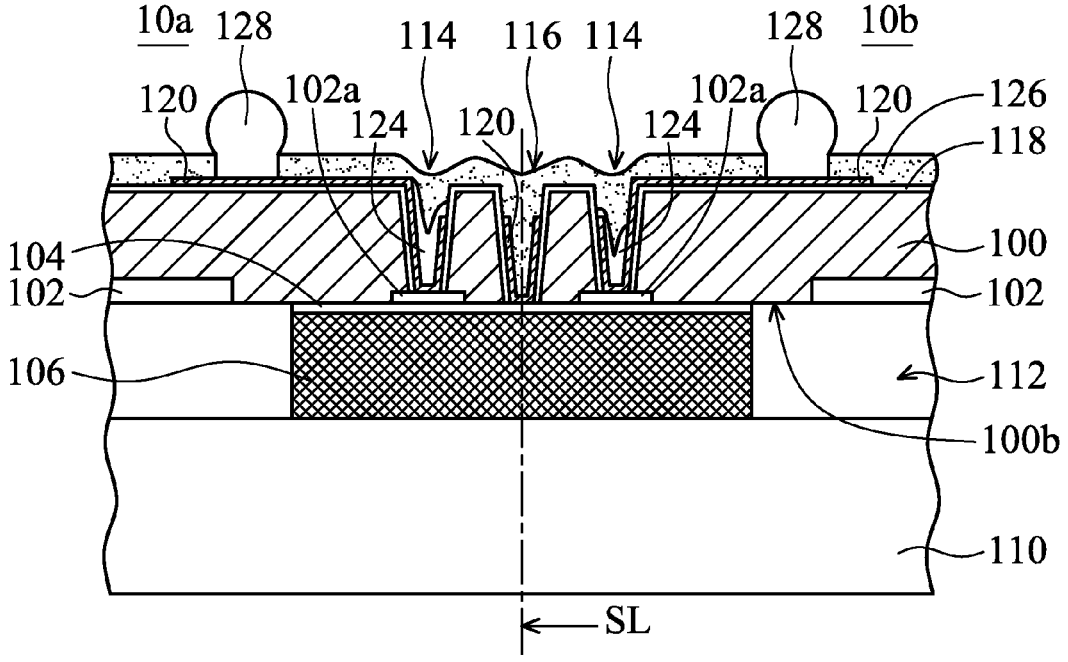
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FIG. 2H

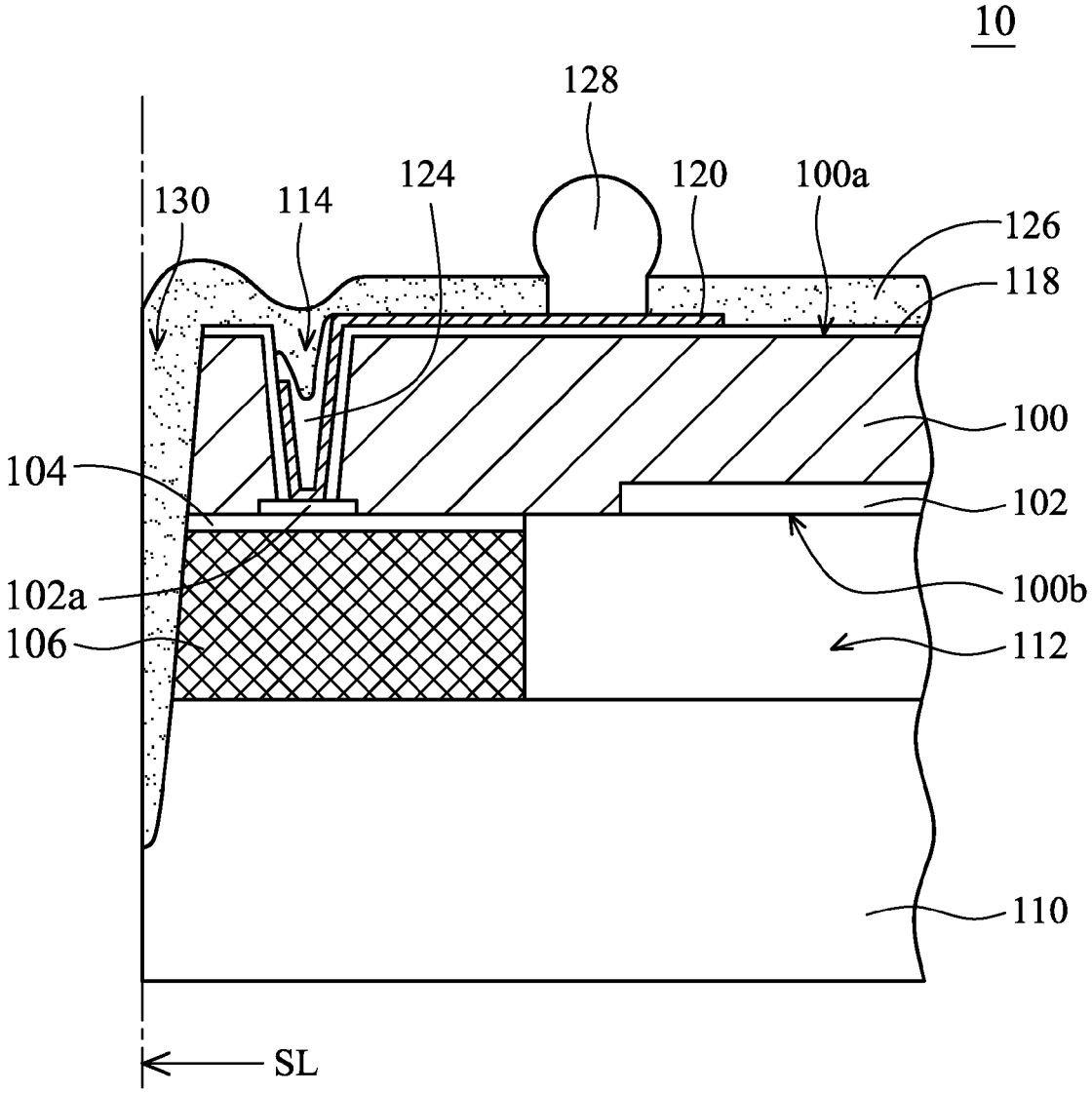
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FIG. 3

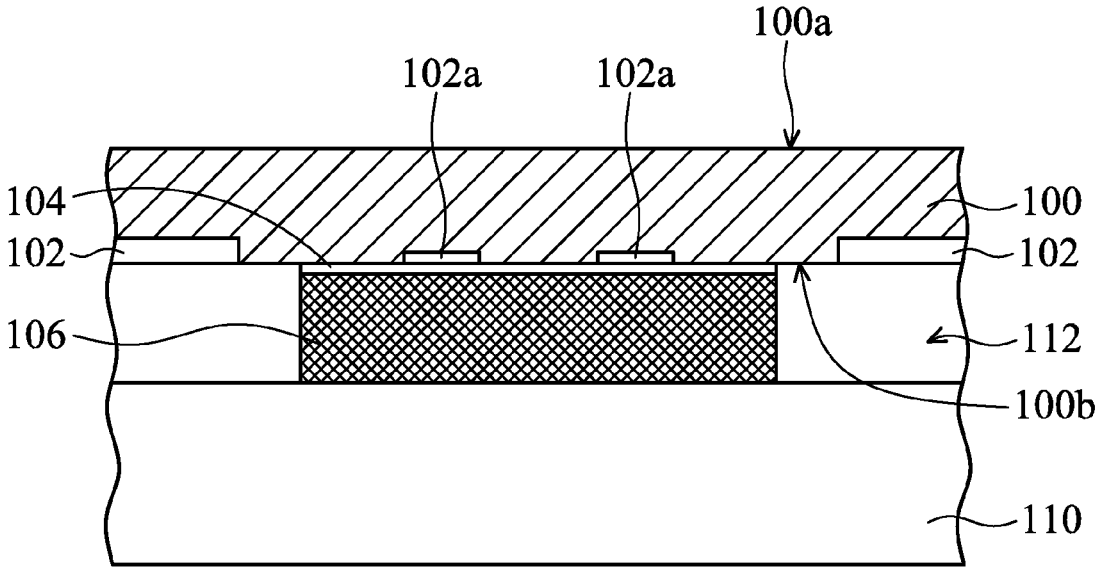
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FIG. 4A

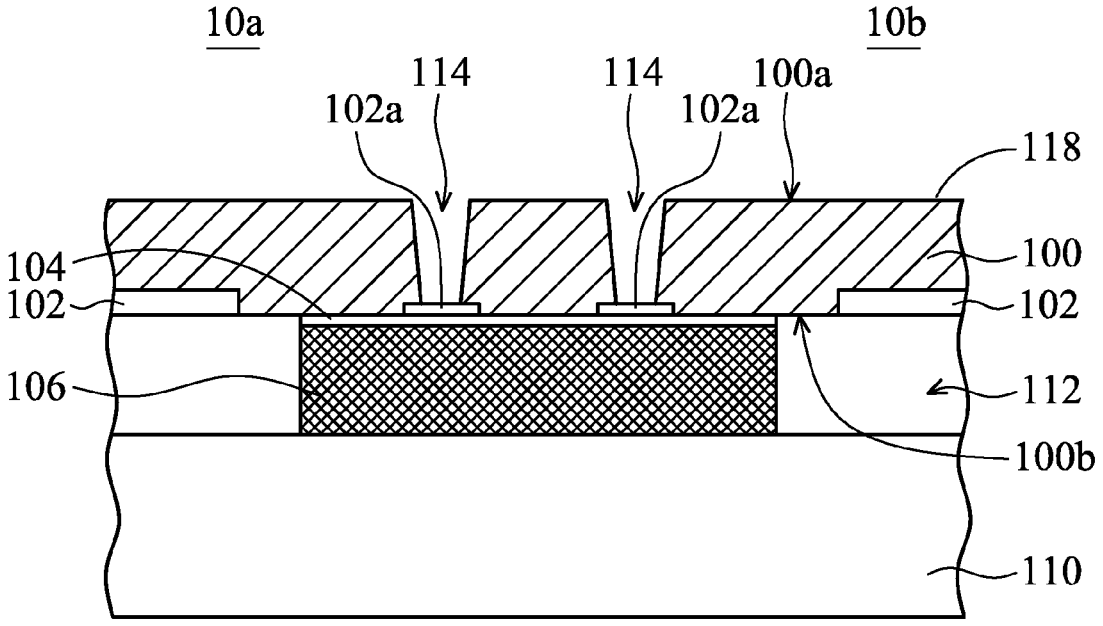
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FIG. 4B

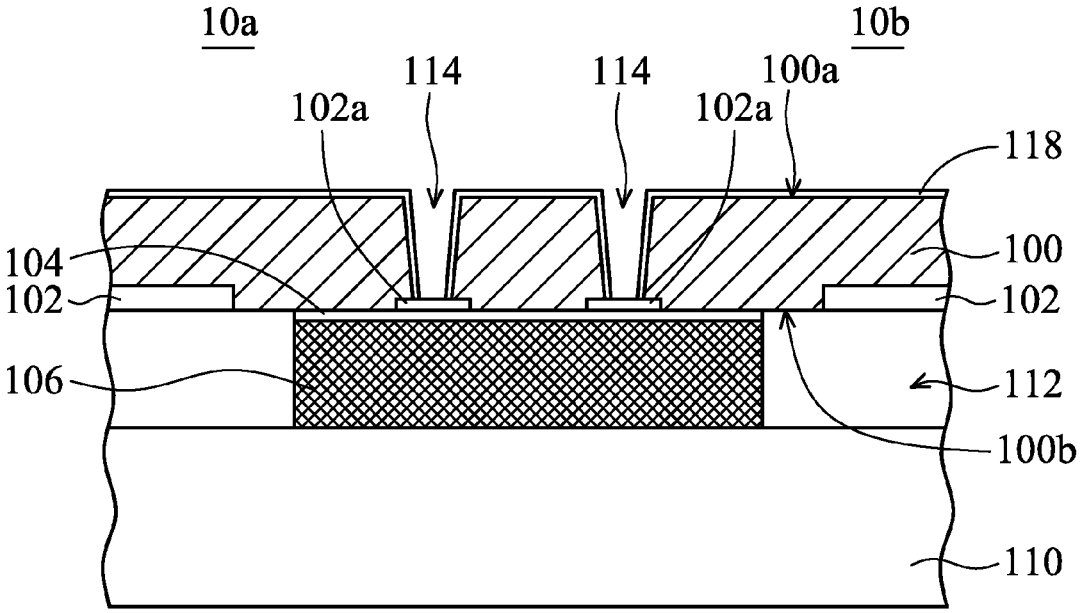
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FIG. 4C

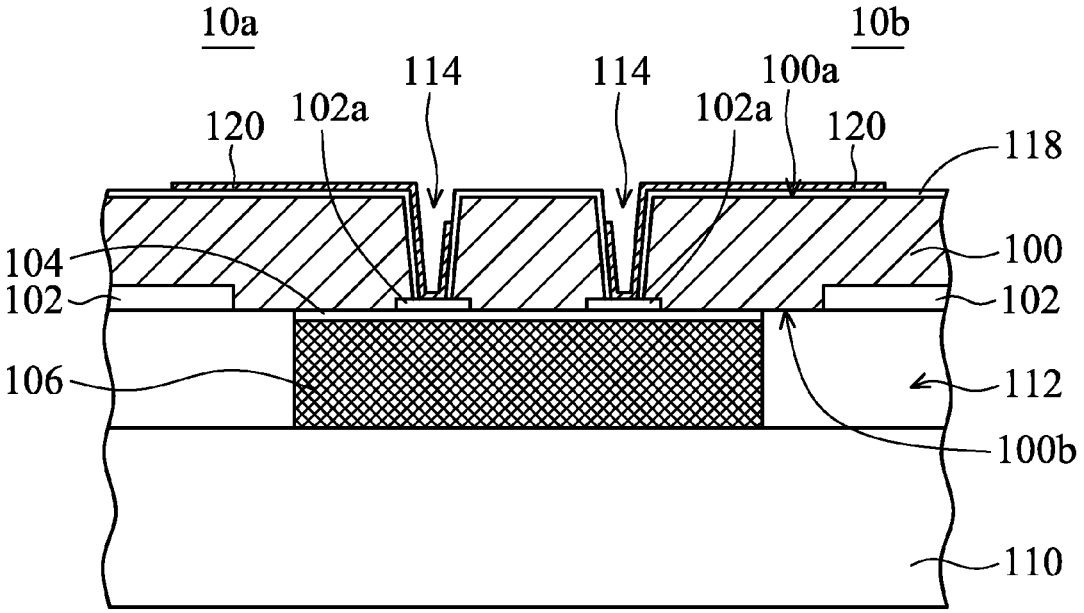
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FIG. 4D

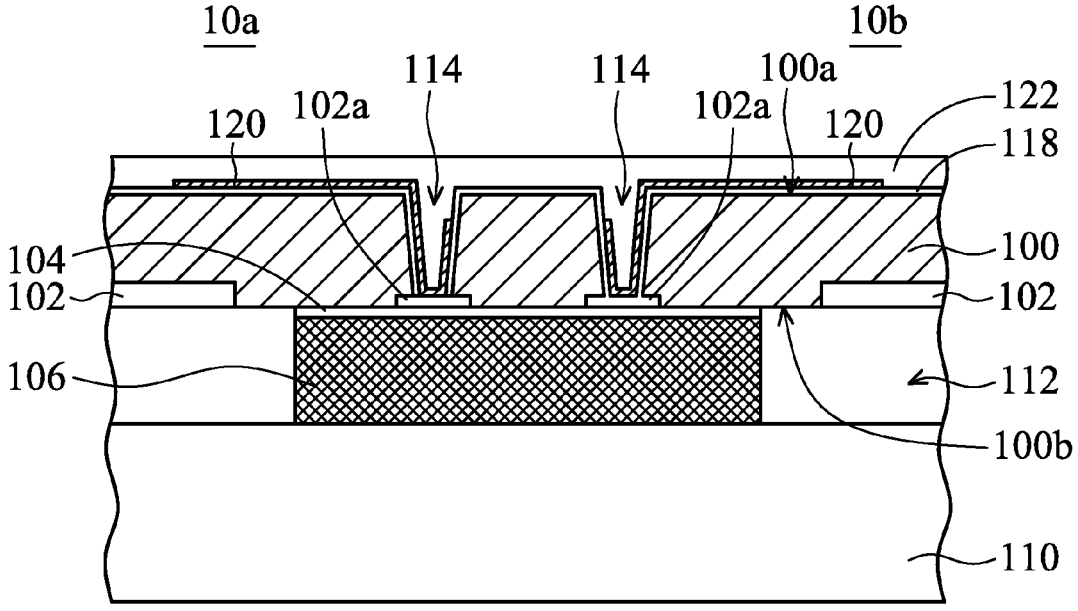
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FIG. 4E

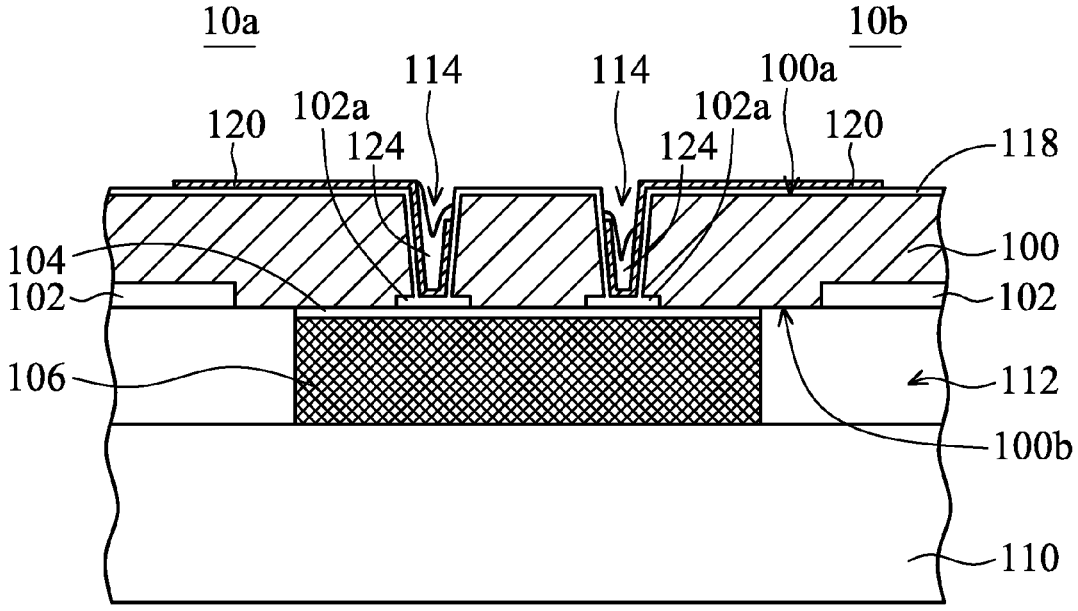
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FIG. 4F

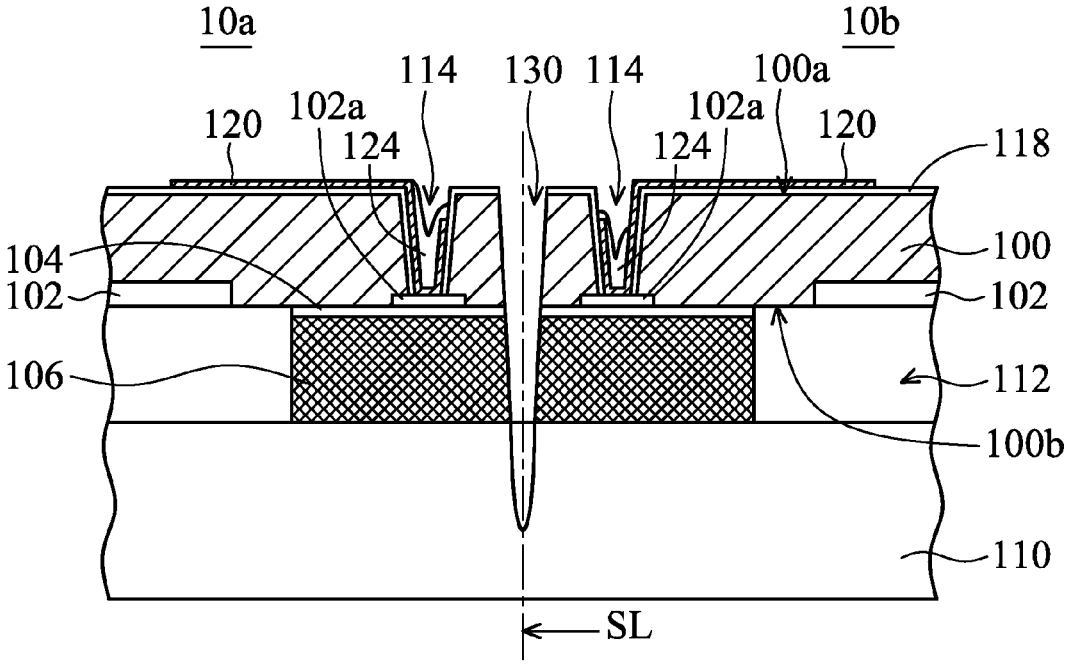
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FIG. 4G

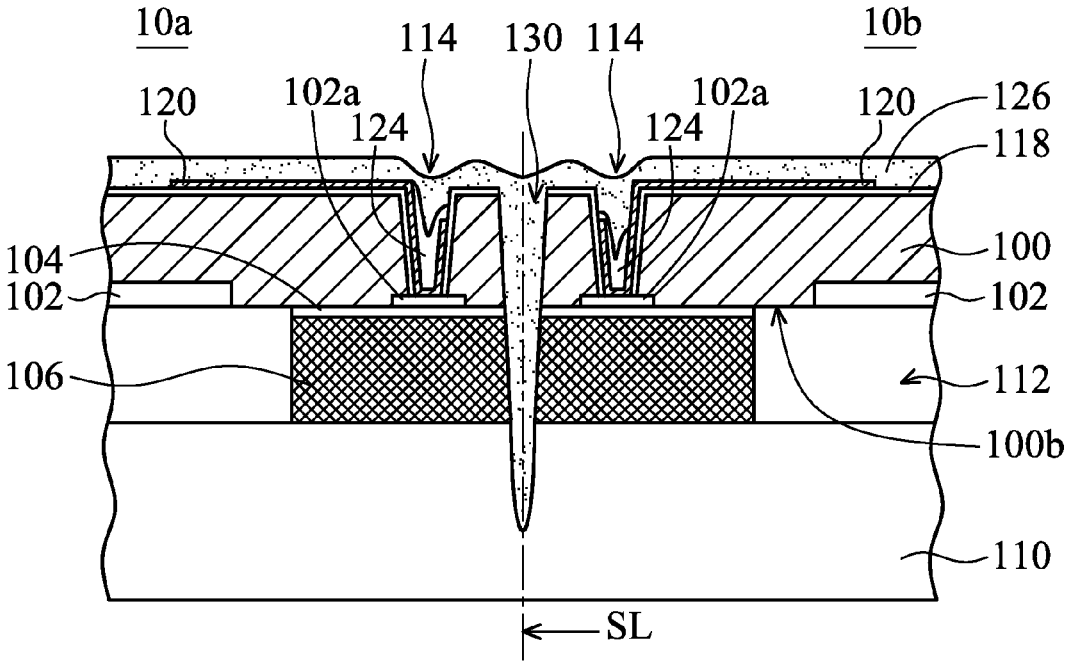
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FIG. 4H

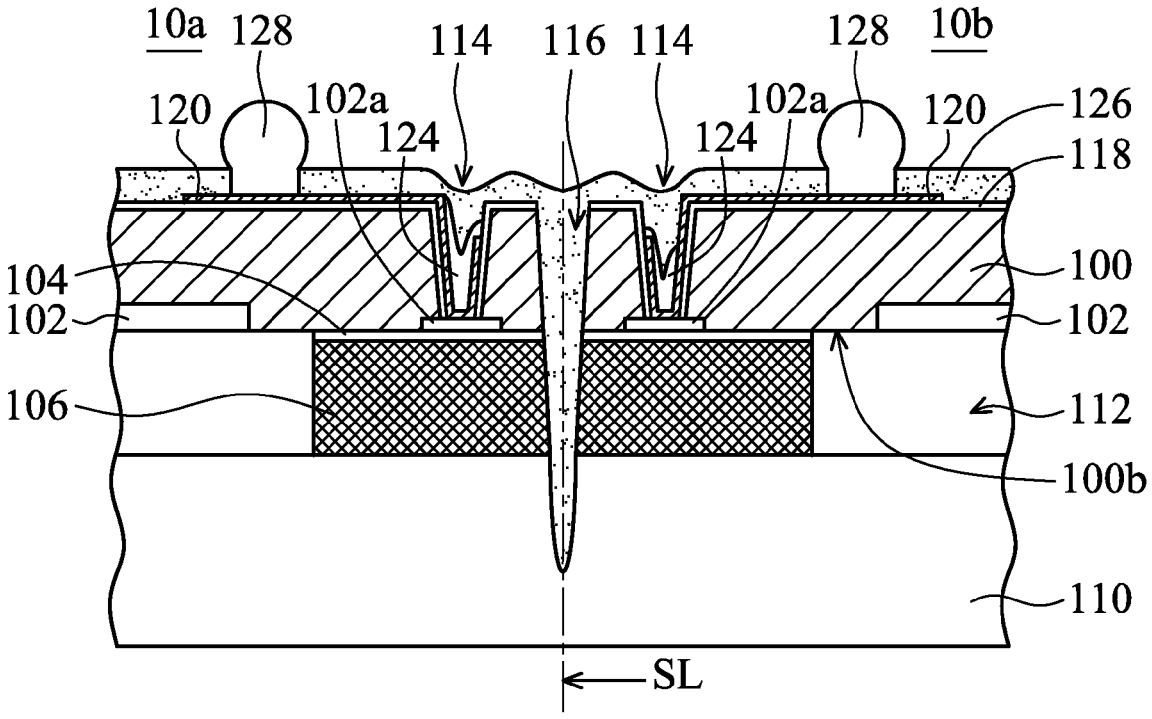
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FIG. 4I

FABRICATION METHODS OF CHIP DEVICE PACKAGES

CROSS REFERENCE TO RELATED APPLICATIONS

This application is a Divisional of pending U.S. patent application Ser. No. 12/816,301, filed Jun. 15, 2010 and entitled "CHIP PACKAGE AND FABRICATION METHOD THEREOF", which is a Continuation-In-Part of pending U.S. patent application Ser. No. 12/687,093, filed Jan. 13, 2010 and entitled "CHIP PACKAGE AND FABRICATION METHOD THEREOF", the entirety of which is incorporated by reference herein.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a chip package, and in particular relates to a chip package with a through-silicon via and a fabrication method thereof.

2. Description of the Related Art

To enable electronic equipment to become smaller, chip packages contained therein have been becoming smaller. One approach for reducing the size of chip packages includes using through-silicon vias in the packaged chips. However, in some situations, a redistribution layer in the through-silicon vias is easily delaminated from the sidewall of the vias during a thermal cycle test. Accordingly, the through-silicon vias also reduce the reliability of the packaged chips.

Thus, a new chip package design and a fabrication method thereof are thus desired.

BRIEF SUMMARY OF THE INVENTION

According to an illustrative embodiment, a chip package is provided. The chip package comprises a semiconductor substrate, having a first surface and an opposing second surface. A through hole is disposed on the first surface, extending from the first surface to the second surface. A conductive trace layer is disposed over the first surface and extends to the through hole. Then, a buffer plug is disposed over the conductive trace layer in the through hole and a protection layer is disposed to cover the entire first surface of the semiconductor substrate.

According to an illustrative embodiment, a method for fabricating a chip package is provided. The method comprises providing a semiconductor substrate, having a first surface and an opposing second surface. Through holes are formed on the first surface, extending from the first surface to the second surface. A conductive trace layer is conformally formed over the first surface and extends to the through holes. Then, a buffer plug is formed over the conductive trace layer in the through holes and a protection layer is formed to cover the entire first surface of the semiconductor substrate.

According to another illustrative embodiment, a chip package is provided. The chip package comprises a semiconductor substrate, having a first surface and an opposing second surface. A spacer is disposed under the second surface of the semiconductor substrate and a cover plate is disposed under the spacer. A recessed portion is formed adjacent to a sidewall of the semiconductor substrate, extending from the first surface of the semiconductor substrate to at least the spacer. Then, a protection layer is disposed over the first surface of the semiconductor substrate and in the recessed portion.

According to another illustrative embodiment, a method for fabricating a chip package is provided. The method comprises providing a semiconductor substrate, having a first surface and an opposing second surface. A spacer is formed under the second surface of the semiconductor substrate. A cover plate is attached to the underside of the spacer. Trench openings are formed on the first surface of the semiconductor substrate along a scribe line, extending from the first surface to at least the spacer. A protection layer is formed over the first surface of the semiconductor substrate and in the trench openings. Then, the semiconductor substrate is diced along the scribe line to form chip packages, wherein each chip package includes at least a recessed portion adjacent to a sidewall of the semiconductor substrate, extending from the first surface of the semiconductor substrate to at least the spacer, and covered with the protection layer.

A detailed description is given in the following embodiments with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention can be more fully understood by reading the subsequent detailed description and examples with references made to the accompanying drawings, wherein:

FIG. **1** shows an illustrative cross section of a chip package according to an embodiment of the invention;

FIGS. **2**A-**2**H are illustrative cross sections showing the steps for fabricating the chip package of FIG. **1** according to an embodiment of the invention;

FIG. **3** shows an illustrative cross section of a chip package according to an embodiment of the invention; and

FIGS. **4**A-**4**I are illustrative cross sections showing the steps for fabricating the chip package of FIG. **3** according to an embodiment of the invention.

DETAILED DESCRIPTION OF THE INVENTION

The following description is of the best-contemplated mode of carrying out the invention. This description is made for the purpose of illustrating the general principles of the invention and should not be taken in a limiting sense. The scope of the invention is best determined by reference to the appended claims.

The embodiments of chip packages of the invention and fabrication methods thereof are illustrated by embodiments of fabricating image sensor chip packages in the following description. However, it should be appreciated that the invention may also be applied to forming other semiconductor chips. Therefore, the packages of the embodiments of the invention may be applied to active or passive devices, or electronic components with digital or analog circuits, such as opto electronic devices, micro electro mechanical systems (MEMS), micro fluidic systems, and physical sensors for detecting heat, light, or pressure. Particularly, a wafer level chip scale package (WLCSP) process may be applied to package semiconductor chips, such as image sensor devices, solar cells, RF circuits, accelerators, gyroscopes, micro actuators, surface acoustic wave devices, pressure sensors, and ink printer heads.

The wafer level chip scale package process mentioned above mainly means that after the package process is accomplished during the wafer stage, the wafer with chips is cut to obtain separate independent chip packages. However, in an embodiment of the invention, separate independent chips may be redistributed overlying a supporting wafer and then be packaged, which may also be referred to as a wafer level chip scale package (WLCSP) process. In addition, the above mentioned wafer level chip scale package process may also be

adapted to form chip packages of multi-layered integrated circuit devices by stacking a plurality of wafers having integrated circuits.

Referring to FIG. **1**, a cross section of a portion of a chip package according to an embodiment of the invention is shown, which can be fabricated by a wafer level chip scale package process. First, a chip **10** with a semiconductor substrate **100** is provided. The semiconductor substrate **100** has a first surface **100***a* and an opposing second surface **100***b*. A semiconductor device **102**, such as a CMOS image sensor and/or micro lens, is formed on the second surface **100***b* serving as an active surface. At least a through hole **114** is formed on the first surface **100***a*, extending from the first surface **100***a* toward the second surface **100***b*. At least a conductive pad **102***a* is exposed by the through hole **114**, which is electrically connected to the semiconductor device **102**, for example, through an interconnection. In another embodiment, at least a recessed portion **116** may be further formed adjacent to a sidewall of the semiconductor substrate **100**, extending from the first surface **100***a* toward the second surface **100***b*, wherein the recessed portion **116** is formed by cutting a trench opening at a scribe line SL. The scribe line SL is disposed between any two adjacent chips.

A patterned insulating layer **118** is formed on the first surface **100***a* and extends to the sidewalls of the through hole **114** and the recessed portion **116**. In another embodiment, the portions of the insulating layer **118** on the bottom sides of the through holes **114** are removed. Examples of materials for forming the insulating layer **118** include, but are not limited to an inorganic material such as silicon dioxide or a photosensitive insulating material such as an insulating photo-resist. A patterned conductive trace layer **120** is then conformally formed on the insulating layer **118** over the first surface **100***a* and extends to the through holes **114**. In an embodiment, the conductive trace layer **120** can be a redistribution layer. The conductive trace layer **120** may be a metal layer made of material such as a copper, aluminum, silver, or nickel layer or alloys thereof. In another embodiment, the patterned conductive trace layer **120** may be further conformally formed within the recessed portion **116**, wherein a gap for isolation is formed between the conductive trace layer **120** in the through hole **114** and the recessed portion **116**.

Note that a buffer plug **124** is formed in the through hole **114** and then a protection layer **126** is formed to cover the first surface **100***a* and fill the through hole **114** and the recessed portion **116**. In the through hole **114**, the filled buffer plug **124** is used to separate the conductive trace layer **120** and the later filled protection layer **126**. In the recessed portion **116**, the conductive trace layer **120** is used to separate the protection layer **126** and the later formed spacer **106**. In the embodiments of the invention, the buffer plug **124** may be formed of one or more than one layers of softer materials. The protection layer **126** may be a harder material, such as solder mask.

In one embodiment, to enhance the reliability of the chip package, the material of the buffer plug **124** is not completely cured, such that the adhesion between the buffer plug **124** and the protection layer **126** within the through hole **114** is reduced. For example, a curable buffer plug **124** may be cured under its Glass Transition Temperature (Tg) or for a shorter time, to thereby obtain a soft cured product with poor adhesion. A curing method is arbitrary, and a method of curing by heat, light, electron beam, or the like may be employed. When a thermal cycle test is performed to the chip package, the protection layer **126**, a harder material, may shrink and a pull up force is then produced from the protection layer **126**. However, the soft buffer plug **124** can be deformed to offset the pull up force from the protection layer **126** and prevent the conductive trace layer **120** from delaminating. That is, most of the buffer plugs **124** in through holes **114** in shape or size are different after the above mentioned curing process.

Alternatively, to offset the great difference between the coefficient of thermal expansion (CTE) of the protection layer **126** and that of the insulating layer **118**, according to an embodiment of the invention, the buffer plug **124** has a CTE between a CTE of the protection layer **126** and a CTE of the insulating layer **118**, such that the difference between the CTEs of the protection layer **126** and the insulating layer **118** can be adjusted by the buffer plug **124** to prevent the chip package from delaminating during the thermal cycle test. In one embodiment, the protection layer **126** may have a CTE of about 159 ppm/° C. and the insulating layer **118** may have a CTE of about 54 ppm/° C. Accordingly, the buffer plug **124** may have a CTE between 159 ppm/° C. and 54 ppm/° C. Moreover, in one example, the buffer plug **124** may be formed of more than one layers of photo-resist with more than one kind of material. Accordingly, the buffer plug **124** may have CTEs which gradually changed from 54 ppm/° C. to 159 ppm/° C.

Referring again to FIG. **1**, a cover plate **110** may be attached to the underside of the second surface **100***b* of the semiconductor substrate **100**. The cover plate **110** or the cover plate may be a transparent substrate or a semiconductor substrate. In an embodiment of the invention, a spacer **106** can be disposed between the cover plate **110** and the semiconductor substrate **100** to form a cavity **112** between the cover plate **110** and the semiconductor device **102**, wherein the cavity **112** is surrounded by the spacer **106**. In another embodiment, the spacer **106** can fill up the space between the cover plate **110** and the semiconductor substrate **100** and no cavity would be produced. The spacer **106** may be formed from materials such as epoxy resin, solder mask or any other suitable supporting materials. In addition, an adhesive layer **104** can be used to attach the spacer **106** and the semiconductor substrate **100**, while the spacer **106** is formed on the cover plate **110**. Alternatively, the adhesive layer can be added between the spacer **106** and the cover plate **110**, while the spacer **106** is formed on the semiconductor substrate **100**. The adhesive layer may be a polymer film, or one or more than one of an adhesive such as an epoxy or polyurethane adhesive.

A conductive bump **128** is disposed in an opening of the protection layer **126** on the first surface **100***a* to electrically connect with the conductive trace layer **120**. The conductive bump **128** may be a solder ball or a solder paste.

The conductive trace layer **120** formed in the recessed portion **116** has several advantages. First, as shown in FIG. **1**, the conductive trace layer **120** in the recessed portion **116** is extended to the scribe line SL and covers the sidewall of the semiconductor substrate **100**, such that it can prevent the chip package from being permeated by moisture. Second, the spacer **106** may be formed from the same material of the protection layer **126** such as a solder mask. Meanwhile, if the protection layer is connected with the spacer, the stress produced in the protection layer and the spacer is great. However, according to an embodiment of the invention, the protection layer **126** is separated from the spacer **106** by the conductive trace layer **120** and the adhesive layer **104**, such that the stress produced in the protection layer **126** and the spacer **106** is reduced.

FIGS. **2**A-**2**H show cross sections of parts of the steps for fabricating a chip package according to an embodiment of the invention. Referring to FIG. **2**A, during a foundry stage, a semiconductor substrate **100** such as a wafer with chips is provided first, having a first surface **100***a* and an opposing second surface **100***b*. A plurality of semiconductor devices

102 is formed on the second surface 100*b*. A plurality of conductive pads 102*a* is formed on the second surface 100*b* to electrically connect with each semiconductor device 102.

Next, a packaging stage is performed. In one embodiment, the second surface 100*b* of the wafer 100 is attached to a cover plate 110 serving as a carrier. The cover plate 110 may be formed from glass, quartz, opal, plastic, or other transparent substrates to provide light emission in and out thereto and therefrom. Note that a filter and/or an anti-reflective layer may be selectively formed on the cover plate 110. In one example, a spacer 106 may be formed on the cover plate 110 or the wafer 100 and then attach one to another, such that a cavity 112 is formed between the cover plate 110 and the wafer 100, as shown in FIG. 2A. The cavity 112 is surrounded by the spacer 106, and the material of the spacer 106 may be epoxy resin, solder mask or any other suitable supporting materials, such as an inorganic material or an organic material of polyimide (PI). In order to increase the hermetic seal of the package, an adhesive layer 104 may be added between the spacer 106 and the wafer 100, while the spacer 106 is formed on the cover plate 110. Alternatively, the adhesive layer can be added between the spacer 106 and the cover plate 110, while the spacer 106 is formed on the semiconductor substrate 100. Next, a step of thinning the wafer 100 at the first surface 100*a* can be selectively performed. The thinning process may be an etching, milling, grinding or polishing process.

Referring to FIG. 2B, a plurality of through holes 114 and/or trench openings 116 are formed in the wafer 100, extending along a direction form the first surface 100*a* to the second surface 100*b* by a removing process such as drilling or etching. The conductive pads 102*a* are exposed by the through holes 114. Each trench opening 116 is formed at the scribe line SL between two adjacent chips 10*a* and 10*b* In an embodiment, the through holes 114 and the trench openings 116 can be formed simultaneously by the same etching process. Alternatively, the trench openings 116 may be notches at the scribe line SL formed by a pre-cutting process from a cutter.

Then, referring to FIG. 2C, in order to isolate the semiconductor substrate 100 and subsequently form conductive trace layers, an insulating material can be conformally formed to cover the first surface 100*a* of the semiconductor substrate 100 and extend to sidewalls and bottom sides of the through holes 114 and the trench openings 116. Then, the insulating material can be patterned to remove the portions of the insulating material at the bottom sides of the through holes 114 and the bottom sides of the trench openings 116 to form the patterned insulating layer 118. The conductive pads 102*a* at the bottom sides of the through holes 114 are also exposed by the patterned insulating layer 118. In one embodiment, the insulating layer 118 may be formed from a photosensitive insulating material. In this embodiment, the photosensitive insulating material can be selected from photosensitive organic polymer materials. The compositions of the photosensitive organic polymer materials may include, but is not limited to, a polyimide (PI), butylcyclobutene (BCB), parylene, polynaphthalenes, fluorocarbons, and accrylates material etc. The photosensitive organic polymer materials can be formed by a coating process, such as a spin coating, a spray coating, or a curtain coating process, or other suitable deposition methods.

Referring to FIG. 2D, a conductive material is formed on the entire insulating layer 118. The conductive material is conformally formed over the first surfaces 100*a* of the wafer 100 and extended to the sidewalls and the bottom sides of the through holes 114 and the trench openings 116. In one embodiment, the conductive material may be a copper, aluminum, silver, or nickel layer or alloys thereof, which can be conformally deposited by a physical vapor deposition (PVD) or a sputtering process. Then, the conductive material is patterned by a photolithography and etching process to form the conductive trace layer 120. The conductive trace layer 120 is extended from the first surface 100*a* of the wafer 100 to the sidewalls and the bottom sides of the through holes 114 to electrically connect with the conductive pads at the bottom sides of the through holes 114. The conductive trace layer 120 may be also formed on the sidewalls and the bottom sides of the trench openings 116, but a gap for isolation is formed between the conductive trace layer 120 in the through holes 114 and in the trench openings 116 and thus they are not continuous.

Referring to FIG. 2E, a buffer material 122 is then formed to cover the entire first surface 100*a* of the wafer 100 and fill the through holes 114 and the trench openings 116 by a coating process, such as a spin coating, a spray coating, or a curtain coating process. In an embodiment, the buffer material 122 may be a photosensitive material such as an epoxy based photo resist without fillers. Then, referring to FIG. 2F, the buffer material 122 is patterned by an exposure and a development process to leave a portion of the buffer material 122 in the through holes 114 to form a buffer plug 124. The buffer plug 124 may be a plug in each through hole 114. Then, the buffer plug 124 in the through holes 114 is cured, but not completely, to reduce the adhesion between the buffer plug 124 and subsequently formed protection layer. Therefore, the buffer plug 124 can resist a pull up force from the protection layer during the thermal cycle test and prevent the conductive trace layer 120 in the through holes 114 from delaminating. In addition, because the buffer plug 124 is not completely cured, the buffer plug 124 formed in at least two of the through holes 114 have different shapes at a cross section, for example, one buffer plug 124 in a through hole 114 is different from the other buffer plug 124 in another through hole 114. Moreover, the buffer plug 124 may be formed of one or more than one layers of photosensitive materials.

Referring to FIG. 2G, a protection layer 126 is formed on the conductive trace layer 120, covering the first surface 100*a* of the wafer 100 and filling the through holes 114 and the trench openings 116. The protection layer 126 may be a solder mask with fillers such as silicon carbide, silicon oxide, or aluminum oxide. Note that the buffer plug 124 has a CTE between a CTE of the protection layer 126 and a CTE of the insulating layer 118 or the conductive trace layer 120, such that the difference between the CTEs of the protection layer 126 and the insulating layer 118 or the conductive trace layer 120 can be adjusted by the buffer plug 124 to prevent the chip package from delaminating during the thermal cycle test. In one embodiment, the protection layer 126 may have a CTE of about 159 ppm/° C. and the insulating layer 118 may have a CTE of about 54 ppm/° C. Accordingly, the buffer plug 124 may have a CTE between 159 ppm/° C. and 54 ppm/° C.

Then, referring to FIG. 2H, a conductive bump 128 is formed through the protection layer 126 to electrically connect to the conductive trace layer 120. In an embodiment, after forming the protection layer 126, an opening to expose a portion of the conductive trace layer 120 can be formed by patterning the protection layer 126. Next, a solder is filled into the above mentioned opening by an electroplating or a screen printing method. A re-flow process is performed to form the conductive bump 128 such as a solder ball or a solder paste. Then, the above mentioned wafer scale package is diced along the scribe line SL to separate each chip to form a plurality of the chip packages of FIG. 1.

According to an embodiment of the invention, the trench openings **116** at the scribe line SL is formed by the etching process, such that there is no micro-crack produced in the sidewalls of the semiconductor substrate **100**. In addition, after the dicing process, the recessed portion **116** is thus formed and the conductive trace layer **120** in the recessed portion **116** is extended to the scribe line SL and covers the sidewalls of the semiconductor substrate **100**. Accordingly, the conductive trace layer **120** can effectively prevent the chip package from being permeated by moisture.

Moreover, in an embodiment of the invention, there is no buffer plug in the recessed portion **116**, such that the adhesion of the protection layer **126** in the recessed portion **116** is better than that in the through hole **114** to avoid the delamination of the protection layer **126** in the recessed portion **116**.

Next, referring to FIG. **3**, a cross section of a portion of a chip package according to an embodiment of the invention is shown, which can be fabricated by a wafer level chip scale package process. First, a chip **10** with a semiconductor substrate **100** is provided. The semiconductor substrate **100** has a first surface **100***a* and an opposing second surface **100***b*. A semiconductor device **102**, such as a CMOS image sensor and/or micro lens, is formed on the second surface **100***b* serving as an active surface. At least a through hole **114** is formed on the first surface **100***a*, extending from the first surface **100***a* toward the second surface **100***b*. At least a conductive pad **102***a* is exposed by the through hole **114**, which is electrically connected to the semiconductor device **102**, for example, through an interconnection.

A cover plate **110** is attached to the underside of the second surface **100***b* of the semiconductor substrate **100**. The cover plate **110** may be a transparent substrate or a semiconductor substrate. In an embodiment, a spacer **106** is disposed between the cover plate **110** and the semiconductor substrate **100** to form a cavity **112** between the cover plate **110** and the semiconductor device **102**, wherein the cavity **112** is surrounded by the spacer **106**. In another embodiment, the spacer **106** can fill up the space between the cover plate **110** and the semiconductor substrate **100** so that no cavity is produced. The spacer **106** may be formed from materials such as epoxy resin, a solder mask or any other suitable supporting materials. In addition, an adhesive layer **104** can be used to attach the spacer **106** with the semiconductor substrate **100**, wherein the spacer **106** is formed on the cover plate **110**. Alternatively, the adhesive layer can be added between the spacer **106** and the cover plate **110**, wherein the spacer **106** is formed on the semiconductor substrate **100**. The adhesive layer may be a polymer film, or one or more than one of an adhesive such as an epoxy or polyurethane adhesive additive.

At least a recessed portion **130** may be formed adjacent to a sidewall of the semiconductor substrate **100**, extending from the first surface **100***a* to the spacer **106** or further to the cover plate **110**, wherein the recessed portion **130** is formed by cutting a trench opening at a scribe line SL. The scribe line SL is disposed between any two adjacent chips.

An insulating layer **118** is formed on the first surface **100***a* and extends to the sidewalls of the through holes **114**. The portions of the insulating layer **118** on the bottom sides of the through holes **114** are removed to expose the conductive pad **102***a*. Examples of materials for forming the insulating layer **118** include, but are not limited to an inorganic material such as silicon dioxide or a photosensitive insulating material such as an insulating photo-resist. A patterned conductive trace layer **120** is then conformally formed on the insulating layer **118** over the first surface **100***a* and extends to the through holes **114**, but does not extend to the recessed portion **130**. In an embodiment, the conductive trace layer **120** can be a redistribution layer. The conductive trace layer **120** may be a metal layer made of material such as a copper, aluminum, silver, or nickel layer or alloys thereof.

A buffer plug **124** is formed in the through hole **114** over the conductive trace layer **120** and then a protection layer **126** is formed to cover the first surface **100***a* and fill the through hole **114** and the recessed portion **130**. In the through hole **114**, the filled buffer plug **124** is used to separate the conductive trace layer **120** with the later filled protection layer **126**. In the recessed portion **130**, the protection layer **126** directly covers the sidewalls of the semiconductor substrate **100** and the spacer **106** or further covers the sidewall of the cover plate **110**. In the embodiments, the buffer plug **124** may be formed of one or more than one layer of softer materials. The protection layer **126** may be a harder material, such as a solder mask.

In one embodiment, to enhance the reliability of the chip package, the material of the buffer plug **124** is not completely cured, such that the adhesion between the buffer plug **124** and the protection layer **126** within the through hole **114** is reduced. For example, a curable buffer plug **124** may be cured under its Glass Transition Temperature (Tg) or by a shorter time, to thereby obtain a soft cured product with poor adhesion. The curing method is arbitrarily chosen, and a method for curing by using heat, light, electron beam, or the like may be employed. When a thermal cycle test is performed to the chip package, the protection layer **126**, a harder material, may shrink and a pull up force is then produced from the protection layer **126**. However, the soft buffer plug **124** can be deformed to offset the pull up force from the protection layer **126** and prevent the conductive trace layer **120** in the through hole **114** from delaminating. That is, most of the shapes or sizes of the buffer plugs **124** in the through holes **114** are different after the above mentioned curing process.

Alternatively, to offset the great difference between the coefficient of thermal expansion (CTE) of the protection layer **126** and that of the insulating layer **118**, according to an embodiment of the invention, the buffer plug **124** has a CTE between a CTE of the protection layer **126** and a CTE of the insulating layer **118**, such that the difference between the CTEs of the protection layer **126** and the insulating layer **118** can be adjusted by the buffer plug **124** to prevent the chip package from delaminating during the thermal cycle test. In one embodiment, the protection layer **126** may have a CTE of about 159 ppm/° C. and the insulating layer **118** may have a CTE of about 54 ppm/° C. Accordingly, the buffer plug **124** may have a CTE between 159 ppm/° C. and 54 ppm/° C. Moreover, in one example, the buffer plug **124** may be formed of more than one layers of photo-resist with more than one kind of material. Accordingly, the buffer plug **124** may have CTEs which gradually change from 54 ppm/° C. to 159 ppm/° C.

Then, a conductive bump **128** is disposed in an opening of the protection layer **126** on the first surface **100***a* to electrically connect with the conductive trace layer **120**. The conductive bump **128** may be a solder ball or a solder paste.

The protection layer **126** in the recessed portion **130** covers at least the sidewalls of the semiconductor substrate **100** and the spacer **106** and may further cover the sidewall of the cover plate **110**, such that the interfaces between the semiconductor substrate **100**, the spacer **106** and the cover plate **110**, exposed to an ambient environment, are eliminated. Therefore, preventing the chip package from being permeated by moisture.

FIGS. **4A-4I** show cross sections of parts of the steps for fabricating a chip package according to an embodiment of the invention. Referring to FIG. **4A**, during a foundry stage, a semiconductor substrate **100** such as a wafer with chips is provided first, having a first surface **100***a* and an opposing

second surface **100***b*. A plurality of semiconductor devices **102** is formed on the second surface **100***b*. A plurality of conductive pads **102***a* is formed on the second surface **100***b* to electrically connect with each semiconductor device **102**.

Next, a packaging stage is performed. In one embodiment, the second surface **100***b* of the wafer **100** is attached to a cover plate **110** serving as a carrier. The cover plate **110** may be formed from glass, quartz, opal, plastic, or other transparent substrates to provide light emission in and out thereto and therefrom. A filter and/or an anti-reflective layer may be selectively formed on the cover plate **110**. In one example, a spacer **106** may be formed on the cover plate **110** or the wafer **100** and then attached to one another, such that a cavity **112** is formed between the cover plate **110** and the wafer **100**, as shown in FIG. **4**A. The cavity **112** is surrounded by the spacer **106**, and the material of the spacer **106** may be epoxy resin, solder mask or any other suitable supporting materials, such as an inorganic material or an organic material of polyimide (PI). In order to increase the hermetic seal of the package, an adhesive layer **104** may be added between the spacer **106** and the wafer **100**, wherein the spacer **106** is formed on the cover plate **110**. Alternatively, the adhesive layer can be added between the spacer **106** and the cover plate **110**, wherein the spacer **106** is formed on the semiconductor substrate **100**. Next, a step of thinning the wafer **100** at the first surface **100***a* can be selectively performed. The thinning process may be an etching, milling, grinding or polishing process.

Then, referring to FIG. **4**B, a plurality of through holes **114** is formed in the wafer **100**, extending along a direction from the first surface **100***a* to the second surface **100***b* by a removing process such as drilling or etching process. The conductive pads **102***a* are exposed by the through holes **114**.

Referring to FIG. **4**C, in order to isolate the semiconductor substrate **100** and subsequently form conductive trace layers, an insulating material can be conformally formed to cover the first surface **100***a* of the semiconductor substrate **100** and extend to sidewalls and bottom sides of the through holes **114**. Then, the insulating material can be patterned to remove the portions of the insulating material at the bottom sides of the through holes **114** to form the patterned insulating layer **118**. The conductive pads **102***a* at the bottom sides of the through holes **114** are exposed by the patterned insulating layer **118**. In one embodiment, the insulating layer **118** may be formed from a photosensitive insulating material. In this embodiment, the photosensitive insulating material can be selected from photosensitive organic polymer materials. The compositions of the photosensitive organic polymer materials may include, but is not limited to, a polyimide (PI), butylcyclobutene (BCB), parylene, polynaphthalenes, fluorocarbons, and accrylates material etc. The photosensitive organic polymer materials can be formed by a coating process, such as a spin coating, a spray coating, or a curtain coating process, or other suitable deposition processes.

Referring to FIG. **4**D, a conductive material is formed on the entire insulating layer **118**. The conductive material is conformally formed over the first surfaces **100***a* of the wafer **100** and extending to the sidewalls and the bottom sides of the through holes **114**. In one embodiment, the conductive material may be a copper, aluminum, silver, or nickel layer or alloys thereof, which can be conformally deposited by a physical vapor deposition (PVD) or a sputtering process. Then, the conductive material is patterned by a photolithography and etching process to form the patterned conductive trace layer **120**. The patterned conductive trace layer **120** is extended from the first surface **100***a* of the wafer **100** to the sidewalls and the bottom sides of the through holes **114** to electrically connect to the conductive pads at the bottom sides of the through holes **114**. There is a gap between the patterned conductive trace layers **120** of the two adjacent chips **10***a* and **10***b* for electrical isolation.

Referring to FIG. **4**E, a buffer material **122** is formed to cover the entire first surface **100***a* of the wafer **100** and fill the through holes **114** by a coating process, such as a spin coating, a spray coating, or a curtain coating process. In an embodiment, the buffer material **122** may be a photosensitive material such as an epoxy based photo resist without fillers. Then, referring to FIG. **4**F, the buffer material **122** is patterned by an exposure process and a development process to leave a portion of the buffer material **122** in the through holes **114** to form a buffer plug **124**. The buffer plug **124** may be a plug in each through hole **114**. Then, the buffer plugs **124** in the through holes **114** are cured, but not completely, to reduce the adhesion between the buffer plug **124** and a subsequently formed protection layer. Therefore, the buffer plug **124** can resist a pull up force from the protection layer during the thermal cycle test and prevent the conductive trace layer **120** in the through holes **114** from delaminating. In addition, because the buffer plug **124** is not completely cured, the buffer plugs **124** formed in at least two of the through holes **114** have different shapes at a cross section, for example, one buffer plug **124** in a through hole **114** is different from the other buffer plug **124** in another through hole **114**.

Next, referring to FIG. **4**G, a trench opening **130** is formed along a scribe line SL between two adjacent chips **10***a* and **10***b*. The trench opening **130** may be formed by a pre-cutting process from a cutter, such that the trench opening **130** has an inclined plane on the sidewalls of the semiconductor substrate **100** and the spacer **106** and may be further formed on the sidewall of the cover plate **110**. Moreover, the trench opening **130** has a curved shape at a cross section. In one embodiment, the trench opening **130** may be formed extending from the first surface **100***a* of the semiconductor substrate **100** to any depth of the spacer **106**. In another embodiment, the trench opening **116** may be formed extending from the first surface **100***a* of the semiconductor substrate **100** to any depth of the cover plate **110**.

Then, referring to FIG. **4**H, a protection layer **126** is formed covering the first surface **100***a* of the semiconductor substrate **100** and filling the through holes **114** and the trench openings **130**. The buffer plugs **124** in the through holes **114** are covered with the protection layer **126**, and the sidewalls of the semiconductor substrate **100**, the spacer **106** and the cover plate **110** are also covered with the protection layer **126**. The protection layer **126** may be a solder mask with fillers such as silicon carbide, silicon oxide, or aluminum oxide.

Next, referring to FIG. **4**I, a conductive bump **128** is formed passing through the protection layer **126** to electrically connect to the conductive trace layer **120**. In an embodiment, after forming the protection layer **126**, an opening to expose a portion of the conductive trace layer **120** can be formed by patterning the protection layer **126**. Next, a solder is filled into the above mentioned opening by an electroplating or a screen printing method. A re-flow process is performed to form the conductive bump **128** such as a solder ball or a solder paste. Then, the above mentioned wafer level chip scale package is diced along the scribe line SL to separate each chip to form a plurality of the chip packages of FIG. **3**.

According to an embodiment of the invention, the trench openings **130** at the scribe line SL is formed by the pre-cutting process, such that the trench openings **130** can extend from the first surface **100***a* of the semiconductor substrate **100** to the spacer **106** or further to the cover plate **110**. In addition, after the dicing process, the recessed portion **130** of the chip package is formed and covered with the protection layer **126**.

Accordingly, the protection layer **126** in the recessed portion **130** can effectively prevent the chip package from being permeated by moisture.

Moreover, in an embodiment of the invention, there is no buffer plug in the recessed portion **130**, such that the adhesion of the protection layer **126** in the recessed portion **130** is better than that in the through hole **114** to avoid delamination of the protection layer **126** in the recessed portion **130**.

While the invention has been described by way of example and in terms of the preferred embodiments, it is to be understood that the invention is not limited to the disclosed embodiments. To the contrary, it is intended to cover various modifications and similar arrangements (as would be apparent to those skilled in the art). Therefore, the scope of the appended claims should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements.

What is claimed is:

1. A method for fabricating a chip package, comprising:
- providing a semiconductor substrate, having a first surface and an opposing second surface;
- forming a spacer under the second surface of the semiconductor substrate;
- providing a cover plate to attach under the spacer;
- forming a recessed portion adjacent to a sidewall of the semiconductor substrate, extending from the first surface of the semiconductor substrate to the spacer;
- forming a protection layer over the first surface of the semiconductor substrate and to fill the recessed portion;
- forming a through hole on the first surface of the semiconductor substrate; and
- forming a buffer material in the through hole and covered by the protection layer, wherein the buffer material is different from the material of the protection layer.

2. The method as claimed in claim **1**, wherein the recessed portion is formed to extend from the first surface of the semiconductor substrate and further to the cover plate.

3. The method as claimed in claim **1**, wherein the recessed portion is formed by a pre-cutting process and has an inclined plane, and the protection layer is formed to cover the inclined plane of the recessed portion.

4. The method as claimed in claim **1**, further comprising:
- forming a conductive trace layer, conformally covering the first surface of the semiconductor substrate and in the through hole, wherein the buffer material is formed in the through hole over the conductive trace layer.

5. The method as claimed in claim **4**, further comprising:
- forming an insulating layer between the semiconductor substrate and the conductive trace layer,
- wherein the buffer material has a coefficient of thermal expansion between a coefficient of thermal expansion of the protection layer and a coefficient of thermal expansion of the insulating layer.

6. The method as claimed in claim **1**, wherein the buffer material is softer than the protection layer in the through hole.

7. The method as claimed in claim **1**, wherein the buffer material is made of a photosensitive material.

8. The method as claimed in claim **1**, wherein the buffer material fills at least two through holes and the portions of the buffer material in the at least two through holes have different shapes in cross-section.

9. The method as claimed in claim **1**, wherein no metal line is formed under the protection layer in the recessed portion.

10. The method as claimed in claim **1**, wherein the buffer material does not extend to cover above the first surface of the semiconductor substrate outside of the through hole.

11. The method as claimed in claim **1**, wherein the recessed portion is formed after the step of forming the through hole.

12. A method for fabricating a chip device package, comprising:
- providing a semiconductor substrate, having a first surface and an opposing second surface;
- forming a spacer under the second surface of the semiconductor substrate;
- providing a cover plate to attach under the spacer;
- forming a recessed portion adjacent to a sidewall of the semiconductor substrate, extending from the first surface of the semiconductor substrate to the spacer;
- forming a protection layer over the first surface of the semiconductor substrate and in the recessed portion;
- forming a through hole on the first surface of the semiconductor substrate; and
- forming a buffer material in the through hole to partially fill the through hole, wherein the protection layer covers the buffer material in the through hole, and the buffer material does not extend to cover above the first surface of the semiconductor substrate outside of the through hole.

13. A method for fabricating a chip device package, comprising
- providing a semiconductor substrate, having a first surface and an opposing second surface;
- forming a spacer under the second surface of the semiconductor substrate;
- providing a cover plate to attach under the spacer;
- forming a recessed portion adjacent to a sidewall of the semiconductor substrate, extending from the first surface of the semiconductor substrate to the spacer;
- forming a protection layer over the first surface of the semiconductor substrate and in the recessed portion;
- forming a through hole on the first surface of the semiconductor substrate;
- forming a conductive trace layer, conformally covering the first surface of the semiconductor substrate and in the through hole; and
- forming a buffer material in the through hole over the conductive trace layer, wherein the protection layer covers the buffer material in the through hole, and the buffer material does not extend to cover above the first surface of the semiconductor substrate outside of the through hole.

14. The method as claimed in claim **13**, wherein the buffer material is made of a non-conductive material.

15. The method as claimed in claim **13**, wherein the buffer material is softer than the protection layer in the through hole.

16. The method as claimed in claim **13**, further comprising:
- forming an insulating layer between the semiconductor substrate and the conductive trace layer,
- wherein the buffer material has a coefficient of thermal expansion between a coefficient of thermal expansion of the protection layer and a coefficient of thermal expansion of the insulating layer.

17. The method as claimed in claim **13**, wherein buffer material is made of a photosensitive material.

18. The method as claimed in claim **13**, wherein the buffer material fills at least two through holes to form a first buffer plug and a second buffer plug respectively, and the first and second buffer plugs in the at least two through holes have different shapes in cross-section.

19. The method as claimed in claim **18**, wherein the first and second buffer plugs are formed by an exposure and development process to remove the portions of the buffer material outside of the at least two through holes.

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